CATEGORY 4—COMPUTERS

Notes:

1. Computers, related equipment and "software" performing telecommunications or "local area network" functions must also be evaluated against the performance characteristics of Category 5, Part 1 (Telecommunications). *(L.N. 132 of 2001)*
2. Control units which directly interconnect the buses or channels of central processing units, 'main storage' or disk controllers are not regarded as telecommunications equipment described in Category 5, Part 1 (Telecommunications). *(L.N. 85 of 2023)*

   N.B.:

   For the control status of "software" specially designed for packet switching, see Category 5D001 (Telecommunications). *(L.N. 132 of 2001)*

   Technical Note:

   'Main storage' is the primary storage for data or instructions for rapid access by a central processing unit. It consists of the internal storage of a "digital computer" and any hierarchical extension to the "digital computer", such as cache storage or non-sequentially accessed extended storage. *(L.N. 85 of 2023)*
3. *(Repealed L.N. 89 of 2021)*

4A SYSTEMS, EQUIPMENT AND COMPONENTS

4A001 Electronic computers and related equipment, as follows, and "electronic assemblies" and specially designed components therefor:

N.B.: (L.N. 226 of 2009)

See also 4A101.

(a) Specially designed to have any of the following characteristics:

(1) Rated for operation at an ambient temperature below 228 K (-45°C) or above 358 K (85°C);

Note:

4A001(a)(1) does not apply to computers specially designed for civil automobile, railway train or "civil aircraft" applications. *(L.N. 161 of 2011)*

(2) Radiation hardened to exceed any of the following specifications:

(a)	Total Dose	5×10^3 Gy (Si);
(b)	Dose Rate Upset	5×10^6 Gy (Si)/s; *or (L.N. 65 of 2004)*
(c)	Single Event Upset	1×10^{-8} Error/bit/day; *(L.N. 161 of 2011)*

Note:

4A001(a)(2) does not apply to computers specially designed for "civil aircraft" applications. *(L.N. 161 of 2011)*

(b) Deleted; *(L.N. 45 of 2010)*

N.B.:

(Repealed L.N. 85 of 2023)

4A002 Deleted; *(L.N. 65 of 2004)*

4A003 "Digital computers", "electronic assemblies", and related equipment therefor, as follows, and specially designed components therefor:

Notes:

1. 4A003 includes the following:
   (a) 'Vector processors'; *(L.N. 85 of 2023)*
   (b) Array processors;
   (c) Digital signal processors;
   (d) Logic processors;
   (e) Equipment designed for "image enhancement";
   (f) *(Repealed L.N. 89 of 2021)*
2. The control status of the "digital computers" and related equipment described in 4A003 is determined by the control status of other equipment or systems provided:
   (a) The "digital computers" or related equipment are essential for the operation of the other equipment or systems;
   (b) The "digital computers" or related equipment are not a "principal element" of the other equipment or systems; *and*

   N.B.:

   1. The control status of "signal processing" or "image enhancement" equipment specially designed for other equipment with functions limited to those required for the other equipment is determined by the control status of the other equipment even if it exceeds the "principal element" criterion.
   2. For the control status of "digital computers" or related equipment for telecommunications equipment, see Category 5, Part 1 (Telecommunications).

   (c) The "technology" for the "digital computers" and related equipment is determined by 4E.

(a) *(Repealed L.N. 89 of 2013)*

(b) "Digital computers" having an "Adjusted Peak Performance" ("APP") exceeding 70 Weighted TeraFLOPS (WT); *(L.N. 95 of 2006; L.N. 45 of 2010; L.N. 89 of 2013; L.N. 27 of 2015; L.N. 89 of 2021; L.N. 85 of 2023)*

(c) "Electronic assemblies" specially designed or modified for enhancing performance by aggregation of processors so that the "APP" of the aggregation exceeds the limit in 4A003(b); *(L.N. 183 of 1999; L.N. 95 of 2006)*

Notes:

1. 4A003(c) applies only to "electronic assemblies" and programmable interconnections not exceeding the limit in 4A003(b), when shipped as unintegrated "electronic assemblies". *(L.N. 183 of 1999; L.N. 95 of 2006; L.N. 89 of 2021)*
2. 4A003(c) does not control "electronic assemblies" specially designed for a product or family of products whose maximum configuration does not exceed the limit of 4A003(b).

(d) Deleted; *(L.N. 65 of 2004)*

(e) Deleted;

N.B.:

For "electronic assemblies", modules or equipment, performing analogue-to-digital conversions, see 3A002(h). *(L.N. 89 of 2021)*

(f) *(Repealed L.N. 183 of 1999)*

(g) Equipment specially designed for aggregating the performance of "digital computers" by providing external interconnections that allow communications at unidirectional data rates exceeding 2.0 Gbyte/s per link; *(L.N. 45 of 2010)*

Note:

4A003(g) does not apply to internal interconnection equipment (e.g. backplanes, buses), passive interconnection equipment, "network access controllers" or "communications channel controllers". *(L.N. 183 of 1999; L.N. 45 of 2010)*

4A004 Computers, as follows, and specially designed related equipment, "electronic assemblies" and components therefor:

(a) "Systolic array computers";

(b) "Neural computers";

(c) "Optical computers";

4A005 Systems, equipment, and components for the systems and equipment, specially designed or modified for the generation, command and control or delivery of "intrusion software";

(L.N. 27 of 2015; L.N. 89 of 2021)

4A101 Analogue computers, "digital computer" or digital differential analysers, other than those controlled by 4A001(a)(1), which are ruggedized and designed or modified for use in space launch vehicles controlled by 9A004 or sounding rockets controlled by 9A104;

(L.N. 183 of 1999; L.N. 95 of 2006; L.N. 89 of 2021)

4A102 Hybrid computers specially designed for modelling, simulation or design integration of space launch vehicles controlled by 9A004 or sounding rockets controlled by 9A104; *(L.N. 183 of 1999; L.N. 95 of 2006; L.N. 89 of 2021)*

Note:

4A102 only applies when the equipment is supplied with "software" controlled by 7D103 or 9D103.

(L.N. 85 of 2023)

4B TEST, INSPECTION AND PRODUCTION EQUIPMENT

None

4C MATERIALS

None

4D SOFTWARE

Note:

The status of "software" for equipment described in other Categories is dealt with in the appropriate Category. *(L.N. 45 of 2010; L.N. 89 of 2013)*

4D001 "Software" as follows: *(L.N. 89 of 2013)*

(a) "Software" specially designed or modified for the "development" or "production" of equipment or "software" specified in 4A or 4D; *(L.N. 89 of 2013)*

(b) "Software", other than that controlled by 4D001(a), specially designed or modified for the "development" or "production" of:

(1) "Digital computers" having an "Adjusted Peak Performance" ("APP") exceeding 15 Weighted TeraFLOPS (WT); *or (L.N. 226 of 2009; L.N. 45 of 2010; L.N. 27 of 2015; L.N. 42 of 2017; L.N. 89 of 2021)*

(2) "Electronic assemblies" specially designed or modified for enhancing performance by aggregation of processors so that the "APP" of the aggregation exceeds the limit in 4D001(b)(1); *(L.N. 65 of 2004; L.N. 95 of 2006)*

4D002 *(Repealed L.N. 42 of 2017)*

4D003 Deleted; *(L.N. 45 of 2010)*

N.B.:

(Repealed L.N. 85 of 2023)

4D004 "Software" specially designed or modified for the generation, command and control or delivery of "intrusion software";

Note:

4D004 does not apply to "software" specially designed and limited to provide "software" updates or upgrades meeting all of the following:

(1) The update or upgrade operates only with the authorization of the owner or administrator of the system receiving it;

(2) After the update or upgrade, the "software" updated or upgraded is not any of the following:

(a) "Software" specified in 4D004;

(a) "Intrusion software".

(L.N. 89 of 2021)

4E TECHNOLOGY

4E001 (a) "Technology" according to the General Technology Note, for the "development", "production" or "use" of equipment or "software" controlled by 4A or 4D; *(L.N. 65 of 2004)*

(b) "Technology", according to the General Technology Note, other than that controlled by 4E001(a), for the "development" or "production" of: *(L.N. 89 of 2021)*

(1) "Digital computers" having an "Adjusted Peak Performance" ("APP") exceeding 15 Weighted TeraFLOPS (WT); *or (L.N. 226 of 2009; L.N. 45 of 2010; L.N. 27 of 2015; L.N. 42 of 2017; L.N. 89 of 2021)*

(2) "Electronic assemblies" specially designed or modified for enhancing performance by aggregation of processors so that the "APP" of the aggregation exceeds the limit in 4E001(b)(1); *(L.N. 65 of 2004; L.N. 95 of 2006)*

(c) "Technology" for the "development" of "intrusion software"; *(L.N. 27 of 2015)*

Notes:

1. 4E001(a) and 4E001(c) do not control "vulnerability disclosure" or "cyber incident response".

2. Note 1 does not diminish the rights of the competent authority of the country in which the exporter is established to ascertain compliance with 4E001(a) and 4E001(c). *(L.N. 85 of 2023)*

Technical Notes:

(Repealed L.N. 85 of 2023)

TECHNICAL NOTE ON "ADJUSTED PEAK PERFORMANCE" ("APP")

"APP" is an adjusted peak rate at which "digital computers" perform 64-bit or larger floating point additions and multiplications.

Abbreviations used in this Technical Note:

n	number of processors in the "digital computer"
i	processor number (i, . . . n)
t_i	processor cycle time ($t_i = 1/F_i$)
F_i	processor frequency
R_i	peak floating point calculating rate
W_i	architecture adjustment factor

"APP" is expressed in Weighted TeraFLOPS (WT), in units of 10^{12} adjusted floating point operations per second.

Outline of the "APP" calculation method:

1. For each processor i, determine the peak number of 64-bit or larger floating point operations, FPO_i, performed per cycle for each processor in the "digital computer".

Note:

In determining FPO, include only 64-bit or larger floating point additions or multiplications or both. All floating point operations must be expressed in operations per processor cycle; operations requiring multiple cycles may be expressed in fractional results per cycle. For processors not capable of performing calculations on floating point operands of 64-bits or more, the effective calculating rate R is zero.

2. Calculate the floating point rate R for each processor

   $R_i = FPO_i/t_i$

3. Calculate "APP"

   "APP" = $W_1 \times R_1 + W_2 \times R_2 + ... + W_n \times R_n$

4. For 'vector processors', $W_i = 0.9$. For non-'vector processors', $W_i = 0.3$.

Notes:

1. For processors that perform compound operations in a cycle, such as addition and multiplication, each operation is counted.

2. For a pipelined processor, the effective calculating rate R is the faster of the pipelined rate, once the pipeline is full, or the non-pipelined rate.

3. The calculating rate R of each contributing processor is to be calculated at its maximum value theoretically possible before the "APP" of the combination is derived. Simultaneous operations are

assumed to exist when the computer manufacturer claims concurrent, parallel, or simultaneous operation or execution in a manual or brochure for the computer.

4. Do not include processors that are limited to input/output and peripheral functions (e.g. disk drive, communication and video display) when calculating "APP". *(E.R. 6 of 2020)*

5. "APP" values are not to be calculated for processor combinations interconnected by "Local Area Networks", Wide Area Networks, Input/Output shared connections/devices, Input/Output controllers and any communication interconnection implemented by "software".

6. "APP" values must be calculated for processor combinations containing processors specially designed to enhance performance by aggregation, operating simultaneously and sharing memory. *(L.N. 42 of 2017)*

   Technical Notes:

   1. Aggregate all processors and accelerators operating simultaneously and located on the same die.
   2. Processor combinations share memory when any processor is capable of accessing any memory location in the system through the hardware transmission of cache lines or memory words, without the involvement of any "software" mechanism. Processor combinations may be achieved using "electronic assemblies" specified in 4A003(c). *(L.N. 89 of 2013, L.N. 42 of 2017)*

7. A 'vector processor' is defined as a processor with built-in instructions that perform multiple calculations on floating-point vectors (one-dimensional arrays of 64-bit or larger numbers) simultaneously, and having at least 2 vector functional units and at least 8 vector registers of at least 64 elements each.

   (L.N. 95 of 2006)